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AK3918AV100 Series Processors Feature List

Contact Information

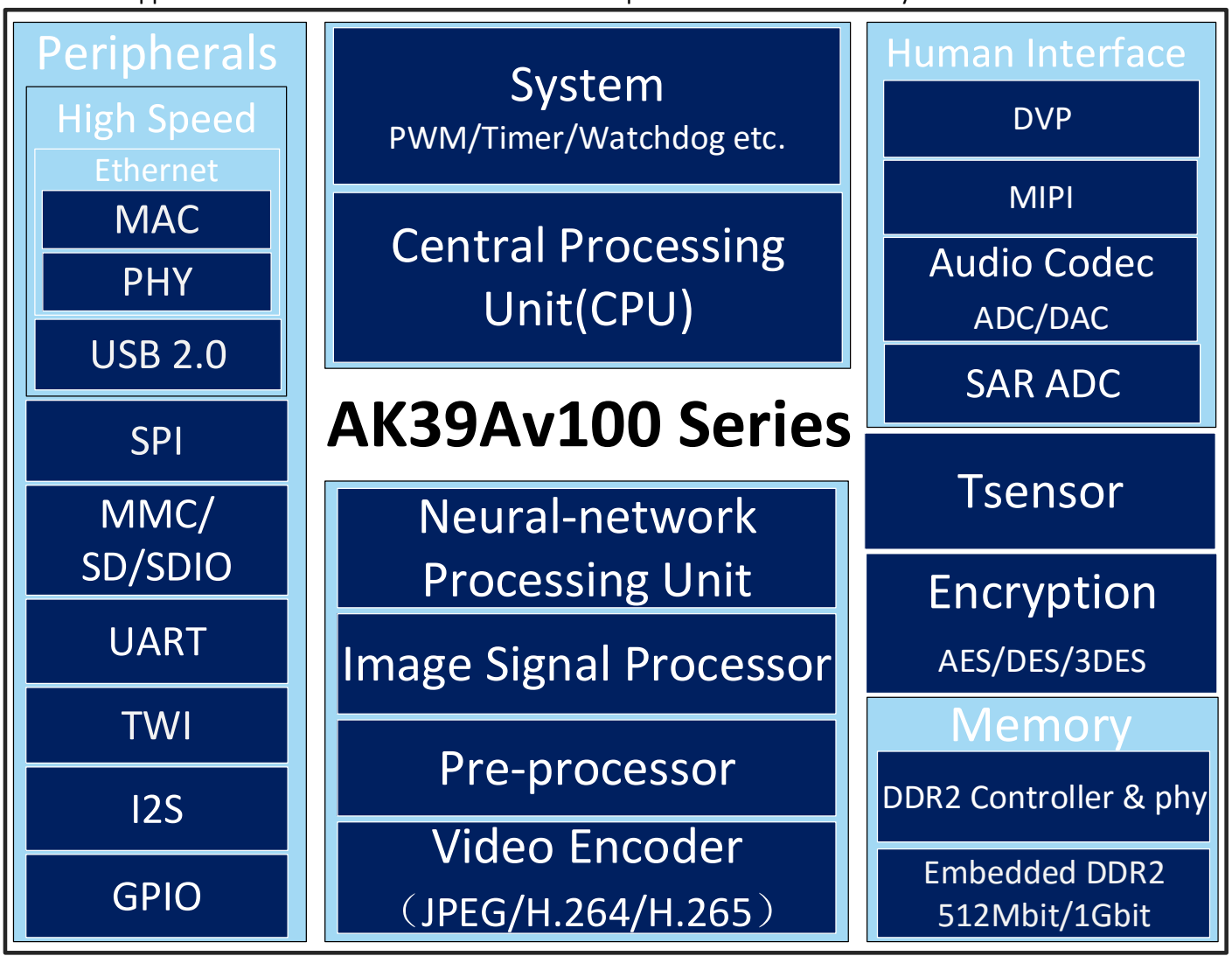
Tel: +86-20-3221-9000
Fax: +86-20-3221-9258
Home Page:
Http://www.anyka.com

Sales Hotline:
+86-20-3221-9499
E-mail:
Sales@anyka.com

AK3918AV100 is specially designed for Internet of Things camera (IoT Camera) applications, one of the key components of cost-sensitive electronic surveillance system.

With the intelligent NPU (Neural-network Processing Unit), the optimized image signal processing algorithm and hardware H.265/H.264 encoder, AK3918AV100 provides an enhanced object detection/tracking and face detection/recognition ability with high quality pictures and low bit rate video encoding at minimal power consumption. It also supports security boot for a better security level. A set of peripheral interfaces, such as UART, SPI, MMC/SD/SDIO, Ethernet MAC and USB2.0, feature AK3918AV100 with high extensibility and high flexibility. Meanwhile, the integrated Fast Ethernet PHY transceiver can reduce the cost of bill-of-materials (BOM) of the final products.

Product Development Kit, including hardware development kit (HDK), software development kit (SDK) and tools, for IoT Camera applications is available for customers to develop in a most convenient way.



CPU

- ARM926EJ-S 32-bit RISC CPU
- Up to 900MHz working frequency
- Supports JTAG interface for development and debugging

Bootstrap

- Supports Normal boot and Security boot
  - Serial NOR Flash Boot
  - SPI NAND Flash Boot
  - eMMC Boot
  - USB Mass Storage Boot
  - UART Boot

Neural-network Processing Unit (NPU)

- Neural network acceleration engine
- Multiple applications such as object detection/tracking and face detection/recognition

Camera Interface

- Supports DVP interface
  - Compatible with BT.601/BT.656/BT.1120 standard
  - Input data width: 8-bit/10-bit
  - Bayer RAW data, YUV422 data, and JPEG compressed data
- Supports 1/2-lane MIPI interface
  - Compliant with MIPI Alliance Standard for Camera Serial Interface 2(CSI-2)
  - Input data width: 8-bit/10-bit/12-bit
  - Bayer RAW data, YUV422 data, YUV420 data, JPEG compressed data and other commonly-used data
- Supports input/output resolution up to 2880*2880

Image Signal Processor (ISP)

- 3A (AWB, AE, AF)
- Gamma correction, color enhancement
- Defect pixel correction
- Lens shading correction
- Noise reduction, blue fringing removal, and green balance
- White balance correction
- 3D/2D noise reduction
- Motion detection
- Edge enhancement
- Sharpening, false color suppression
- Brightness/Contrast adjustment
- Luma transmit improvement

Pre-Processor

- 3 independent channels
- Mirroring and flipping of input image
- OSD and rectangle drawing

Video Processor

- H.265/H.264 encoding of multiple streams:
  - Supports output resolution up to 3072*2048
  - 2880*1620@15fps+640*480@15fps+320*240@15fps+3072*2048@1fps
  - 2304*1296@25fps+640*480@25fps+320*240@25fps+2304*1296@1fps JPEG
  - 1920*1080@30fps+640*480@30fps+320*240@30fps+1920*1080@1fps JPEG
- H.265 encoder
  - Standard: MP Level 1~5
  - Bit rate: VBR, CBR
- H.264 encoder
  - Standard: BP level 1~5/MP Level 1~5/HP level 1~5
  - Bitrate: VBR, CBR
- JPEG encoder
  - Standard: baseline profile (DCT sequential)
  - Supports resolution up to 16384*8192

Ethernet

- 10/100Mbps full-duplex/half-duplex mode
- Compliant with IEEE 802.3az-2010 (EEE)/10Base-T IEEE 802.3/ 100Base-TX IEEE 802.3u
- Supports Auto-Negotiation/ Auto-MDIX

RTC

- Internal simulated RC oscilation
- Supports time counter (second, minute, hour) and calendar counter (day, month, year)
- Supports 12/24-hour mode and leap year mode

Fast SPI Controller (SPI0)

- One SPI master interface for SPI NOR Flash or SPI NAND Flash
- Up to 100MHz working frequency
- Supports Standard SPI, Dual SPI, and Quad SPI

USB Host/Slave

- Supports one USB 2.0 High Speed Host & Slave interface
- Supports high-speed (480Mbps) mode and full-speed (12Mbps) mode
- Supports Control, Bulk, Interrupt and Isochronous transfers

Security Engine

- Hardware AES, DES and 3DES engine

MMC/SD/SDIO

- Three interfaces for eMMC/SD/SDIO/SDHC/micro-SD cards
- Compliant with eMMC/MMC4.2, SD2.0 and SDIO2.0 profile

Tsensor

- Supports chip temperature monitoring
- Supports threshold interrupt and sample completion interrupt

Audio Codec

- One 22-bit Sigma-Delta DAC
- One 16-bit Sigma-Delta ADC

SAR ADC

- One 12-bit SAR ADC
- Two channels
  - keypad input
  - analog-to-digital conversion

Peripheral Interfaces

- Hardware TWI (two-wire interface)
- I2S
- UART (one with hardware flow control)
- GPIO
- PWM
- SPI

Operating Voltage

- IO: 3.3V
- Core: 0.8V
- Image sensor: 1.8V/3.3V
- DDR2 SDRAM: 1.5V

Stacked DDR2 SDRAM

- 512Mbit/1Gbit

Package

- 88-pin QFN package with 9.00mm x 9.00mm x 0.90mm, 0.35mm pitch